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RE: NREL Subcontract # ADJ-1-30630-12

Dear Ken,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of September 9, 2005 to October 9, 2005, under the subject subcontract. The report highlights progress and results obtained under Task 3 (Si-based Solar Cells).

Task 3: Si-Based Solar Cells
This report focuses on the topics of Si based materials development and in-line process diagnostics and control.

Si-based materials development

In the monthly report for March 2005, a design of experiment (DOE) approach was described to continue the study of aluminum induced crystallization (AIC) of Al-Si bilayers. A matrix of samples was created to investigate key variables that had been identified by previous AIC studies at IEC. We are looking for the effect of different structures (normal and reverse), different annealing temperature (above and below eutectic), and annealing time on AIC. The experiments were designed to evaluate the effects of 3 factors on AIC as shown in Table I.

Table I. High and low values of parameters for DOE study of AIC

Name	Low value	High value
Temperature:	450 ^{o}C (<Eu.T)	600 ^{o}C (>Eu.T)

Time:	1hr	6 hr
Structure:	Normal (500nm a-Si/ 400nm Al /substrate 1737)	Reverse (400nmAl/ 500nm a-Si / substrate 1737)

The DOE approach indicated a matrix of 8 samples shown in Table II. Si and Al layers are deposited by e-beam. In both normal and reverse structure, the a-Si layer is 500nm, and the Al layer is 400nn. Since the e-beam system can hold 9 substrates per run, additional substrates were added to the matrix, including mono and multi c-Si wafers, and ceramic.

Presently, all the samples have been deposited and have received the AIC anneal. A sequence of 3 cycles of alternating Al etching in H_3PO_4 and a-Si or nc-Si etching in XeF_2 is in progress to reveal the underlying c-Si layer. Some measurements listed are performed either before, during or after etching: optical microscopy (OM), XRD, AFM, Raman and SEM. Here we report some preliminary results. The following table lists the sample structure and AIC anneal conditions

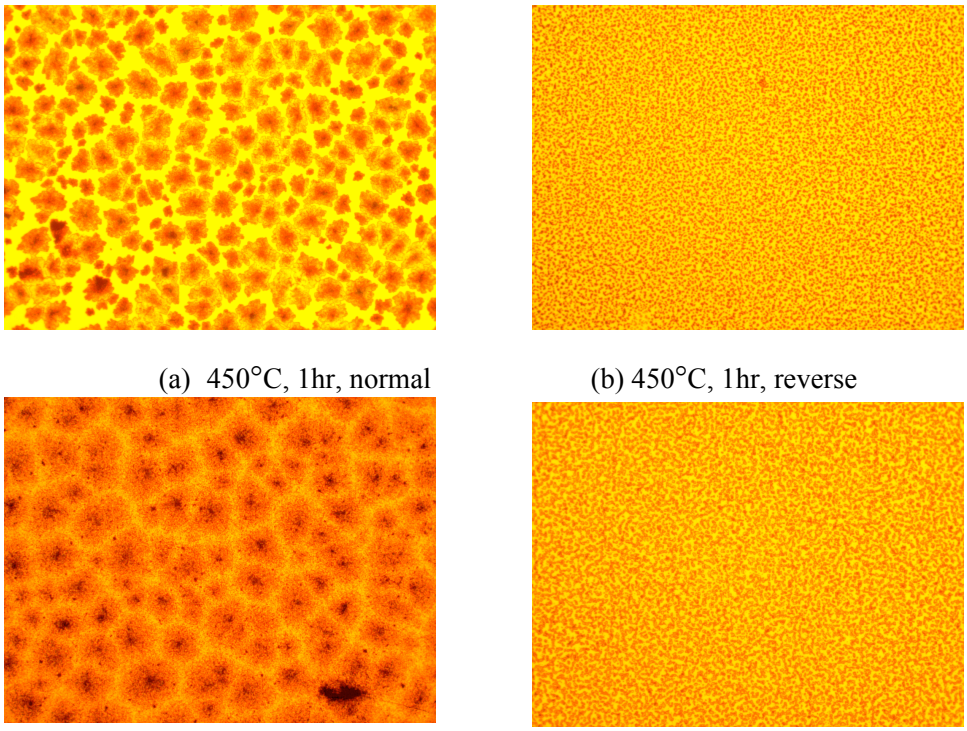
Table II. Matrix of samples and annealing conditions

Anneal Condition		Sample Structure (Normal Si/Al/1737 Reverse Al/Si/1737)
Temperature	Time	
450^{o}C	1hr	normal
450^{o}C	1hr	reverse
450^{o}C	6hr	normal
450^{o}C	6hr	reverse
600^{o}C	1hr	normal
600^{o}C	1hr	reverse
600^{o}C	6hr	normal
600^{o}C	6hr	reverse

The measurements <u>before the etching</u> shows:

a. For samples annealed at 450^{o}C, we got the expected result: dendritic shape crystallites of silicon. One hr was insufficient to complete the AIC; after 6 hrs, all the crystallized silicon regions are connected according to OM, with "grain" size ~20um. We are not sure if these "grains" are pure crystalline silicon or they are composed of many small nano-silicon regions. We need to do etching to reveal the c-Si layer.

b. For reverse structure sample annealed @450^{o}C, from OM measurement, the nucleation density is much larger than the normal structure, and the "grain" of silicon is smaller. The layer exchange speed is slow; even after 6 hrs, the fraction of area with crystallization is still small. (see Figure 1)



(a) 450°C, 1hr, normal (b) 450°C, 1hr, reverse

(c) 450°C, 6hr, normal (d) 450°C, 6hr, reverse

Figure 1 OM of different structures annealed at 450°C. (a) 1hr, normal; large disconnected regions of Si ;(b) 450°C, 1hr, reverse; compared with (a), the nucleation density is larger, and "grain" size is smaller; (c) 450°C, 6 hr, normal; the "grains" are all connected and (d) 450°C, 6 hr, reverse, the percentage c-Si is still small.

c. There was no difference between annealing at 600°C for 1 hr or 6 hr for the normal structure, but for reverse structure samples, crystallization increases with the longer time 6hrs, which can seen from XRD result (Figure 2), where the Si (111) peak is higher, and no Al peak is detected for the 6 hr annealing sample.

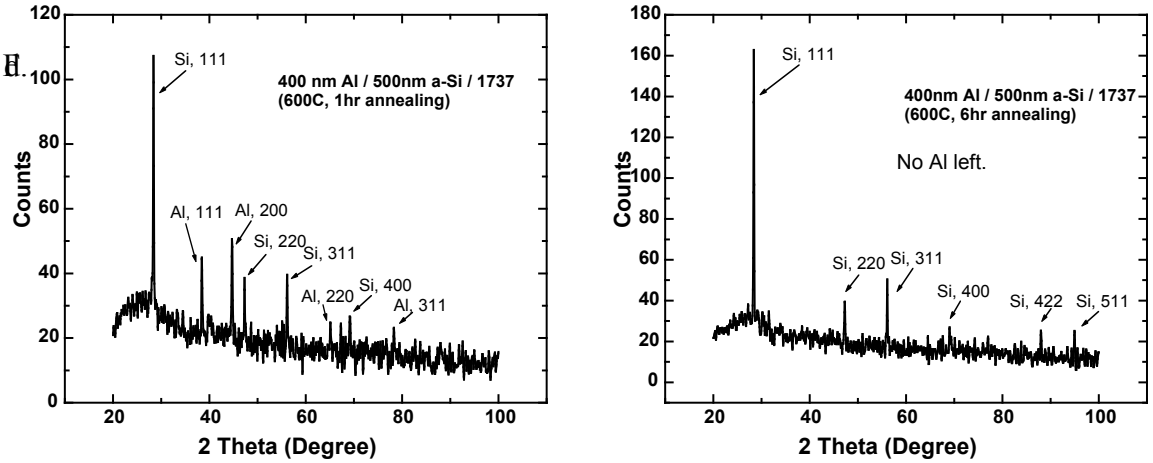


Figure 2. XRD scans of normal structure at 600°C for 1 hr (left) and 6 hr (right).

d. For the normal structure, Figures 3a and 3b show that annealing at 600°C for 1 hr results in a much stronger XRD Si (111) peak, compared to samples annealed at 450°C for the same time. The Si (111) signal is an order of magnitude larger and the Al signal is greatly decreased. While the SEM shows the "grains" (more accurately "regions") are large, over 100 um, they are non-uniform in appearance. The EDS measurement on the sample annealed at 600°C shows most of the grains are a mixture of Al and Si, which appears to contradict the XRD data. Since the Si and Al melted, it is possible that there are Si grains imbedded in an amorphous Si-Al alloy.

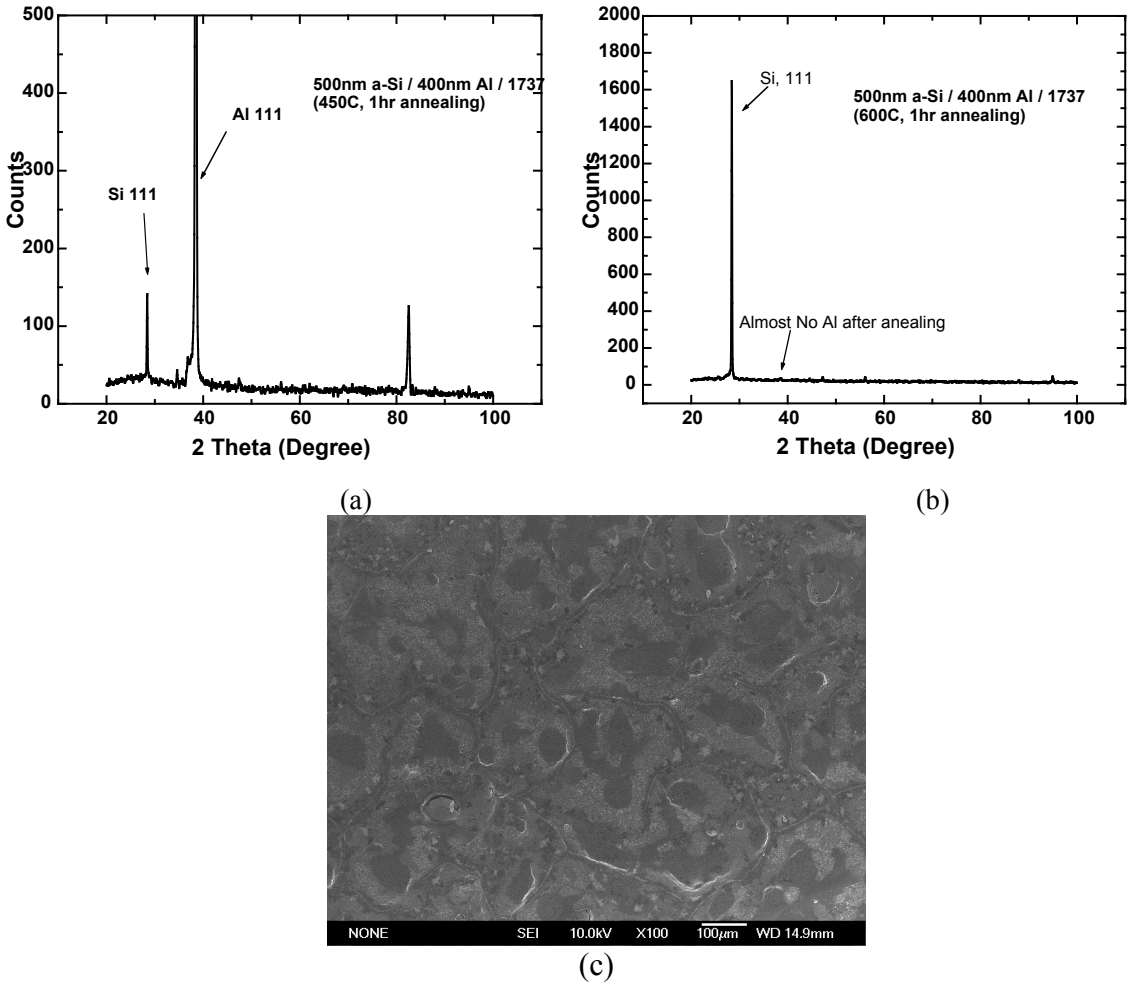


Figure 3 (a) XRD of normal structure annealed at 450°C for 1 hr; (b) XRD of normal structure annealed at 600°C for 1 hr. The Si (111) peak is much stronger; and (c) SEM of normal structure annealed at 600°C for 1hr. The different color in each big "grain" (region) shows non-uniform, also EDS shows most of them are Si-Al mixture.

e. Raman measurement indicates a much stronger c-Si peak for reversed samples as expected. Layer inversion would leave their Si layer on top while it is on the bottom for normal structure, and Raman measurements are more sensitive to the surface. Etching will remove the Al on top and that will provide a more accurate Raman measurement for normal structure samples.

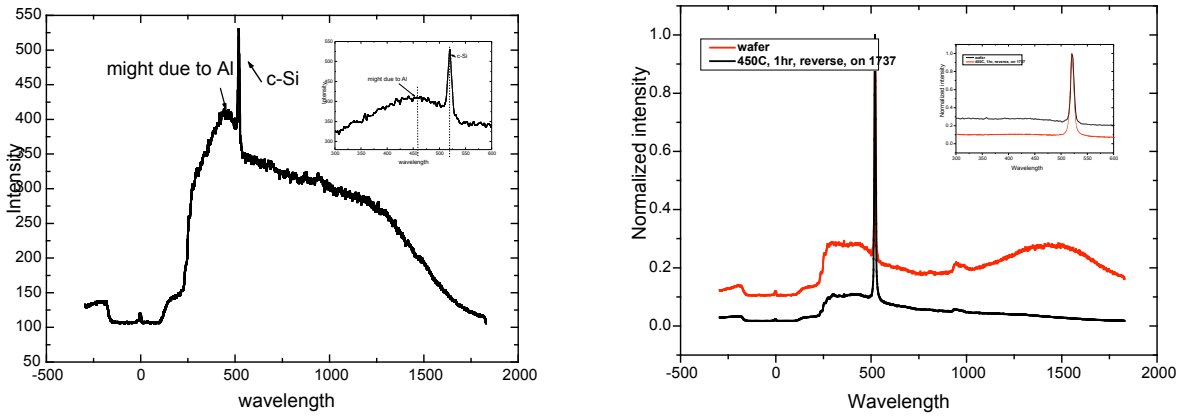


Figure 4. Raman measurement of (a) normal structure (b) reverse structure, both annealed @ 450°C 1hr, before etching.

Tables III and IV shows the samples fabricated on different substrates at 450° and 600°C.

Table III. Samples on non-glass substrates annealed below eutectic temperature.

Substrate	Heat Treatment Condition		Sample Structure (Normal: Si/Al/sub Reverse: Al/Si/sub)
	Temperature	Time	
wafer	450°C	1hr	normal
wafer	450°C	6hr	normal
ceramic	450°C	1hr	normal
ceramic	450°C	6hr	reverse

Table IV. Samples on non-glass substrates annealed above eutectic temperature.

Substrate	Heat Treatment Condition		Sample Structure (Normal: Si/Al/sub Reverse: Al/Si/sub)
	Temperature	Time	
c-Si wafer	600°C	1hr	normal
c-Si wafer	600°C	1hr	reverse
c-Si wafer	600°C	6hr	normal
c-Si wafer	600°C	6hr	reverse
mc-Si wafer	600°C	1hr	normal
mc-Si wafer	600°C	6hr	normal
ceramic	600°C	1hr	normal
ceramic	600°C	1hr	reverse
ceramic	600°C	6hr	normal
ceramic	600°C	6hr	reverse

Since samples on these substrates are not transparent, the OM measurement doesn't provide any information. Other measurement shows:

a. For samples on c-Si wafer, XRD shows only Si (100), which is the same orientation as the Si wafer. There were no Si (111) peaks, which normally appear after crystallization for other substrates (see figures above). There are two possibilities: no crystallization exists, or the Si grew epitaxially. We need more research to see which case happened.

b. SEM shows the film on wafer substrate has cracks, which is not seen on other substrates.

c. For each substrate, the trends for time & temperature effects are similar to those on 1737 glass.

d. Based on XRD and the Raman data before etching, it seems the best substrate is for forming a continuous large grain Si layer is 1737 glass, but it still needs to be confirmed by after etching and more measurements.

Selected samples were annealed at even higher temperature, i.e. above 600°C. They show no major difference compared to 600°C samples before etching. This is reasonable since for both 600°C and 700°C, the Si and Al films have melted.

Substrate	Heat Treatment Condition		Sample Structure (Normal Si/Al/1737 Reverse Al/Si/1737)
	Temperature	Time	
ceramic	700°C	6hr	normal
ceramic	700°C	6hr	reverse

To summarize these results of AIC before etching:

1. Temperature effect: Si layer for samples annealed above eutectic temperature (600°C) is continuous for normal structure, and seems to give big "grains" which are a mixture of Al and Si. More measurements are needed for sample after etching to see if it will improve. Annealing above 600°C had no obvious benefit compared to 600°C.
2. Structure effect: The nucleation density is much larger for the reverse structure, and the "grain" of crystallized silicon is smaller, compared to the normal structure.
3. Annealing time effect: As expected, for sample annealed below eutectic temperature (450°C), a longer time (6 hr) gives higher crystallinity. For sample above eutectic temperature, this is also true for reverse structure samples, but not true for normal structure samples.
4. Substrate effect: It seems the best substrate for forming a continuous and big grain Si layer is 1737 glass, but more measurements are needed after etching.

Diagnostics: Process Control for Co-evaporative PVD Process

The performance of a well-designed co-evaporative physical vapor deposition process for CIGS thin-film growth depends mainly on the ease of controlling individual elemental vapor fluxes. This is done essentially by manipulating the individual source-boat temperature set-points provided by a model predictive controller to achieve the desired film thickness and composition. In such a cascaded control structure, fast and accurate inner-loop controllers are essential. The popular PID controllers are usually employed to control the inner temperature loops.

Even though employed widely in industrial practice, the popular PID controller has weaknesses that limit its achievable performance, and an intrinsic structure that makes tuning not only more complex than necessary, but also less transparent with respect to the key attributes of the overall controller performance, namely: robustness, set-point tracking, and disturbance rejection. We have proposed an alternative control scheme[1] that combines the simplicity of the PID controller with the versatility of model predictive control (MPC) while avoiding the tuning problems associated with both. The tuning parameters of the proposed control scheme are related directly to the controller performance attributes; they are normalized to lie between 0 and 1; and they arise naturally from the formulation in a manner that makes it possible to tune the controller directly for each performance attribute independently. The result is a controller that can be designed and implemented much more directly and transparently, and one that outperforms the classical PID controller both in set-point tracking and disturbance rejection while using precisely

the same process reaction curve information required to tune PID controllers. Figure 5 shows how the four tuning parameters directly influence the controller performance attributes of set-point tracking, robustness, disturbance rejection and overall controller aggressiveness.

Placement of thermocouples for source-boat temperature measurement is another important issue directly affecting the performance of temperature controllers. Presently, thermocouples are placed at the bottom-center of the source-boats. Since the heater is placed near the top of an effusion source, any change in the heater-power will immediately affect the melt-surface-temperature, thereby changing the vapor flow rate; the corresponding change in the boat bottom-center temperature is relatively gradual. Hence, it is important to place the temperature sensor in the top-lid for faster response. The issue of thermocouple placement becomes even more problematic if a linear source-boat with three or more nozzles is used because the temperature at the source-center is higher than that of boat-ends. A two-dimensional and, if possible, three-dimensional thermal modeling is necessary to estimate the melt temperature profile. This will allow us not only to infer melt-temperatures under all the nozzles by a single temperature measurement at the top-lid center (and hence to use a simple single-input-single-output controller), but also to determine the nozzle diameters such that equal effusion rates are obtained from multiple nozzles for a given source temperature set-point.

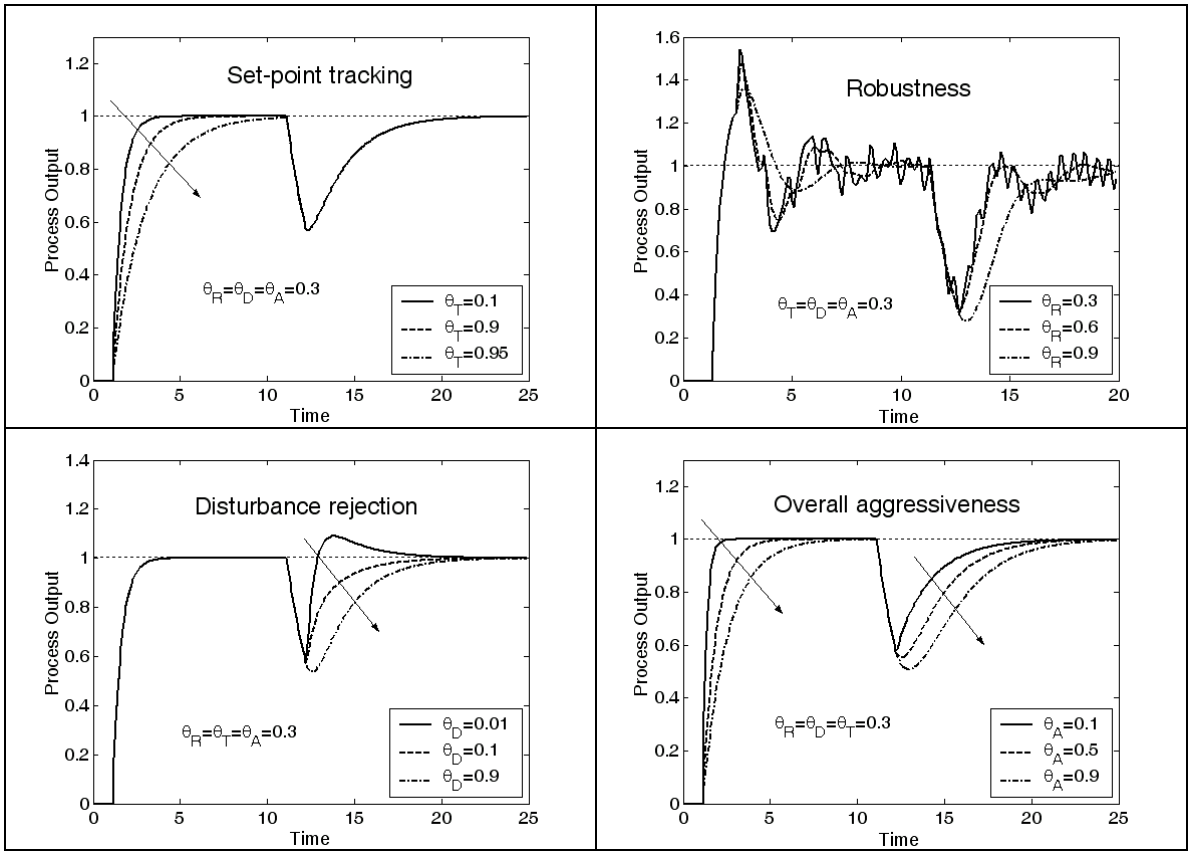


Figure 5: Effect of tuning parameters on controller performance attributes. The arrows indicate the direction of increasing parameter values.

Reference:

[1.] Ogunnaike, B.A. and Mukati, K., "An alternative structure for next generation regulatory controllers. Part I: Basic theory for design, development and implementation," *Journal of Process Control*, In Press, (2005).

Best regards,

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Director

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